SGP-QSFP+SR

40Gbps QSFP SR4 Optical Transceiver Module

Features

- 4 independent full-duplex channels
- Up to 11.2Gbps data rate per channel
- MTP/MPO optical connector
- QSFP MSA compliant
- Digital diagnostic capabilities
- Capable of over 100m transmission on OM3 multi-mode ribbon fiber
- CML compatible electrical I/O
- Single +3.3V power supply
- Operating case temperature: 0~70C
- XLPPI electric interface (with 1.5W Max power)
- RoHS-6 compliant

Applications

- Rack to rack
- Data Center
- Infiniband QDR, DDR and SDR
- 40G Ethernet

1. General Description

The SGP-QSFP-SR4 is a parallel 40Gbps Quad Small Form-factor Pluggable (QSFP) optical module. It provides increased port density and total system cost savings. The QSFP full-duplex optical module offers 4 independent transmit and receive channels, each capable of 10Gbps operation for an aggregate data rate of 40Gbps over 100 meters of OM3 multi-mode fiber.

An optical fiber ribbon cable with an MPO/MTP™ connector can be plugged into the QSFP module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved though a z-pluggable 38-pin IPASS® connector.

SGP-QSFP-SR4 operates by a single +3.3V power supply. LVCMOS/LVTTL global control signals, such as Module Present, Reset, Interrupt and Low Power Mode, are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals, and to receive digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility.

The SGP-QSFP-SR4 is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

2. Functional Description

The SGP-QSFP-SR4 converts parallel electrical input signals into parallel optical signals, by a driven Vertical Cavity Surface Emitting Laser (VCSEL) array. The transmitter module accepts electrical input signals compatible with Common Mode Logic (CML) levels. All input data signals are differential and internally terminated. The receiver module converts parallel optical input signals via a photo detector array into parallel electrical output signals. The receiver module outputs electrical signals are also voltage compatible with Common Mode Logic (CML) levels. All data signals are differential and support a data rates up to 10 Gbps per channel. Figure 1 shows the functional block diagram of the SGP-QSFP-SR4 QSFP Transceiver.

A single +3.3V power supply is required to power up the module. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus – individual ModSelL lines for each QSFP module must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface

and enable the host to access the QSFP memory map.

The ResetL pin enables a complete module reset, returning module settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL (Interrupt) signal with the Data Not Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the module in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a module, is normally pulled up to the host Vcc. When a module is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsL to a "Low" state.

Interrupt (IntL) is an output pin. When"Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

3. Transceiver Block Diagram

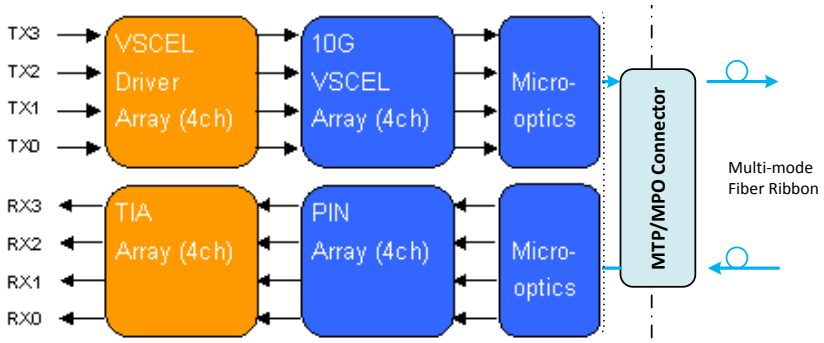


Figure 1：QSFP Transceiver Block Diagram

4. Pin Assignment and Pin Description

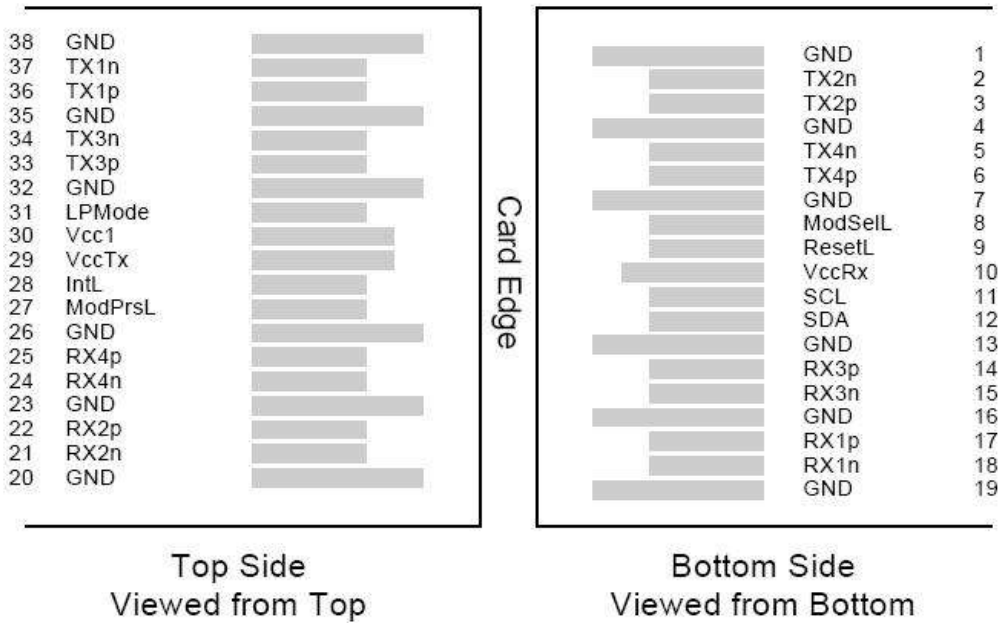


Figure 2: QSFP Transceiver Electrical Pad Layout

5. Pin Definitions

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+ 3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1

17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Note:

1. GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

6. Optical Interface Lanes and Assignment

Figure 3 shows the orientation of the multi-mode fiber facets of the optical connector. Table 1 provides the lane assignment.

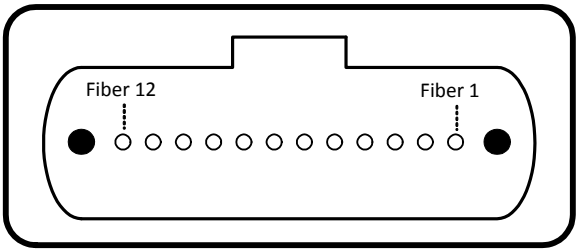


Figure 3: Outside view of the QSFP module MPO receptacle

Table1: lane assignment

Fiber #	Lane Assignment
1	RX0
2	RX1
3	RX2
4	RX3
5	Not used
6	Not used
7	Not used
8	Not used
9	TX3
10	TX2
11	TX1
12	TX0

7. Recommended Power Supply Filter

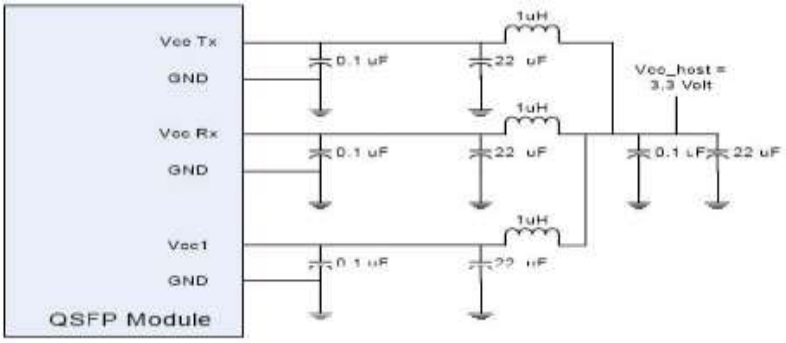


Figure 4 Recommended Power Supply Filter

8. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-20	85	degC	
Relative Humidity (non-condensation)	RH	-	85	%	
Operating Case Temperature	Topc	0	70	degC	1
Supply Voltage	VCC	-0.5	3.6	V	
Voltage on LVTTL Input	Vilvttl	-0.5	VCC+0.5	V	
LVTTL Output Current	Lolvttl	-	15	mA	
Voltage on Open Collector Output	Voco	0	6	V	
Receiver Input Optical Power (Average)	Mip		2	dBm	2

Notes:

1. Ta: -10 to 60degC with 1.5m/s airflow with an additional heat sink.
2. Pin Receiver.

9. Recommended Operating Conditions and Supply Requirements

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Topc	0	70	degC
Power Supply Voltage	VCC	3.1	3.5	V
Power Supply Current	ICC	-	350	mA
Total Power Consumption (XLPPI)		-	1.5	W

10. Optical Characteristics

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Transmitter						
Center Wavelength	λt	840	850	860	nm	
RMS Spectral Width	Pm	-	0.5	0.65	nm	
Average Optical Power, each Lane	Pavg	-8	-2.5	+1	dBm	
Optical Modulation Amplitude (OMA)	Poma	-6	-	+3	dBm	
Peak Power, each Lane	PPt			4	dBm	

Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-7	-		dB	
TDP, each Lane				4	dB	
Extinction Ratio	ER	3	-	-	dB	
Relative Intensity Noise	Rin	-	-	-128	dB/Hz	12dB reflection
Optical Return Loss Tolerance		-	-	12	dB	
Encircled Flux		>86% at 19um <30% at 4.5um				
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		0.23, 0.34, 0.43, 0.27, 0.33, 0.4				
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Receiver						
Center Wavelength	λr	830	850	860	nm	
Damage Threshold	THd	2			dBm	1
Average Power at Receiver Input, each Lane		-9.9		0	dBm	
Receiver Reflectance		-	-	-12	dB	
OMA, each Lane				3	dBm	
Stressed Receiver Sensitivity in OMA, each Lane		-	-	-5.4	dBm	
Receiver Sensitivity per Channel	Psens	-	-13		dBm	
Peak Power, each Lane	PPr			4	dBm	
Receiver Jitter Tolerance Signal Level in OMA, each Lane				-5.4	dBm	

Los Assert	LosA	-30	-	-	dBm	
Los Dessert	LosD	-	-	-14	dBm	
Los Hysteresis	LosH	0.5	-	-	dB	
Overload	Pin	+1	-	-	dBm	
Conditions of Stress Receiver Sensitivity Test[2]:						
Vertical Eye Closure Penalty, each Lane			2		dB	
Stressed Eye J2 Jitter, each Lane			0.35		UI	
Stressed Eye J9 Jitter, each Lane			0.47		UI	
Conditions of Receiver Jitter Tolerance Test:						
Jitter Frequency and Peak-peak Amplitude		(75, 5)			KHz, UI	
		(375,1)				

Notes:

1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

11. DIGITAL DIAGNOSTIC FUNCTIONS

The following digital diagnostic characteristics are defined over the Recommended Operating Environment unless otherwise specified. It is compliant to SFF-8436.

Parameter	Symbol	Min.	Max	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temp
Supply voltage monitor absolute error	DMI_VCC	-0.1	0.1	V	Full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-3	3	dB	Ch1~Ch4

Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	Ch1~Ch4

12. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

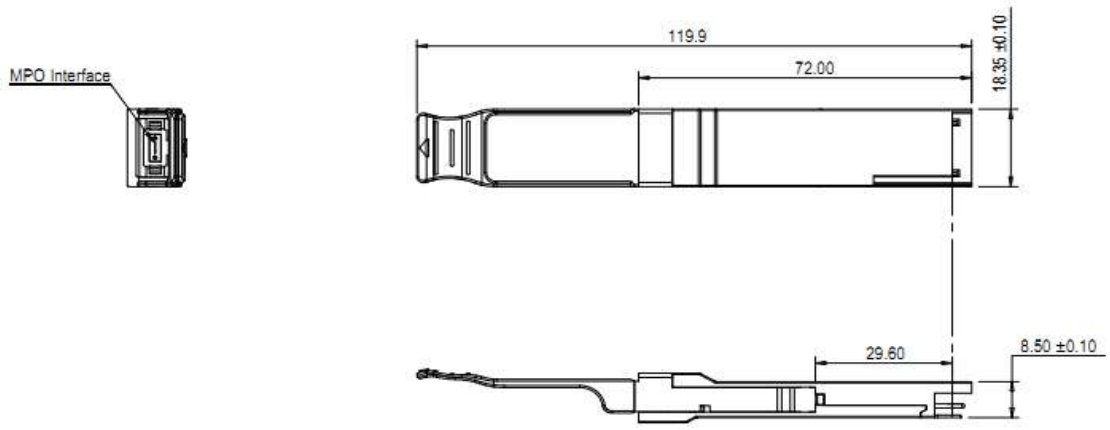
Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Data Rate, each Lane		-	10.3125	11.2	Gbps	
Power Consumption (XLPPI)		-		1.5	W	
Supply Current	ICC		0.75	1.0	A	
Control I/O Voltage, High	VIH	2.0		VCC	V	
Control I/O Voltage, Low	VIL	0		0.7	V	
Inter-Channel Skew	TSK			150	ps	
RESETL Duration			10		us	
RESETL De-assert time				100	ms	
Power on time				100	ms	
Transmitter (XLPPI)						
Single Ended Output Voltage Tolerance		-0.3	-	4	V	Referred to signal common
AC Common mode Voltage Tolerance (RMS)		15	-	-	mV	
Tx Input Diff Voltage	VI	90		1600	mV	
Tx Input Diff Impedance	ZIN	80	100	120	Ω	
Differential Input Return Loss		See IEEE 802.3ba 86A.4.11			dB	10MHz-11.1GHz
J2 Jitter Tolerance	Jt2			0.18	UI	
J9 Jitter Tolerance	Jt9			0.26	UI	
Data Dependent Pulse Width Shrinkage	DDPWS			0.07	UI	
Eye Mask Coordinates {X1, X2 Y1, Y2}		0.1， 0.31 95， 350			UI mV	

Receiver (XLPPI)						
Single Ended Output Voltage Tolerance[1]		-0.3	-	4	V	Referred to TP1 signal common
AC Common mode Voltage Tolerance (RMS)		-	-	7.5	mV	
Termination Mismatch at 1MHz				5	%	
Differential Output Return Loss		See IEEE 802.3ba 86A.4.2.1			dB	10MHz-11.1GHz
Common-mode Output Return Loss		See IEEE 802.3ba 86A.4.2.2			dB	10MHz-11.1GHz
Rx Output Diff Voltage	Vo		600	800	mV	
Rx Output Rise and Fall Time	Tr/Tf			35	ps	20% to 80%
J2 Jitter Tolerance	Jr2			0.46	UI	
J9 Jitter Tolerance	Jr9			0.63	UI	
Eye Mask Coordinates {X1, X2 Y1, Y2}		0.29 , 0.5 150 , 425			UI mV	

Notes:

1. The single ended input voltage tolerance is the allowable range of the instantaneous input signals

13. Mechanical Dimensions



14. ESD

This transceiver is specified as ESD threshold 1KV for SFI pins and 2KV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

15. Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:1993:+A1:1997+A2:2001. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50

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